

74VCX245

Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/R input determines the direction of data flow. The OE input disables both the A and B ports by placing them in a high impedance state.

The 74VCX245 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal (Note 1)
- t_{PD}
3.5 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL})
±24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Leadless DQFN Pb-Free package

Note 1: To ensure the high impedance state during power up and power down, OE_n should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

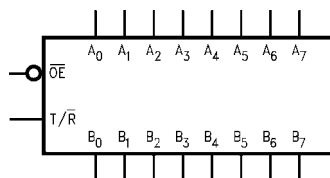
Order Number	Package Number	Package Description
74VCX245WM (Note 2)	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCX245BQX (Note 3)	MLP020B	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74VCX245MTC (Note 2)	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pb-Free package per JEDEC J-STD-020B.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 3: DQFN package available in Tape and Reel only.

Logic Symbol

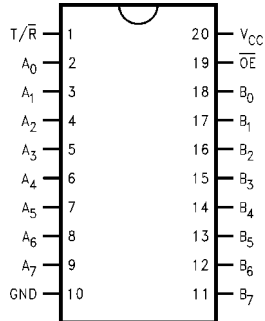


Pin Descriptions

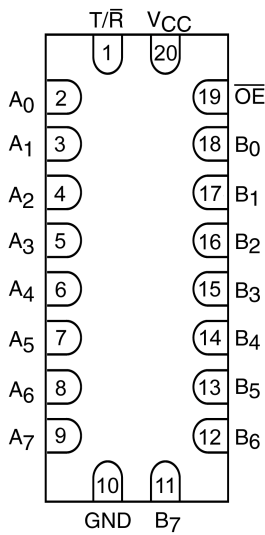
Pin Names	Description
OE	Output Enable Input (Active LOW)
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or 3-STATE Outputs
B ₀ -B ₇	Side B Inputs or 3-STATE Outputs

Connection Diagrams

Pin Assignments for SOIC and TSSOP



Pin Assignment for DQFN



(Top Through View)

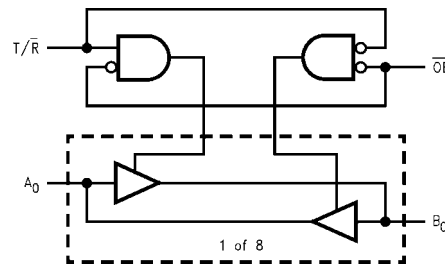
Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇ (Note 4)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Note 4: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 5)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 6)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current	± 100 mA
Storage Temperature (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
$V_{CC} = 1.4V$ to 1.6V	± 2 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 to 3.6	2.0		V
			2.3 to 2.7	1.6		
			1.65 to 2.3	$0.65 \times V_{CC}$		
			1.4 to 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 to 3.6		0.8	V
			2.3 to 2.7		0.7	
			1.65 to 2.3		$0.35 \times V_{CC}$	
			1.4 to 1.6		$0.35 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7 to 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3 to 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65 to 2.3	$V_{CC} - 0.2$		
			1.65	1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 to 1.6	$V_{CC} - 0.2$		
			1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min		Max		Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA I _{OL} = 12 mA I _{OL} = 18 mA I _{OL} = 24 mA	2.7 to 3.6			0.2	V	
			2.7			0.4		
			3.0			0.4		
			3.0			0.55		
		I _{OL} = 100 μA I _{OL} = 12 mA I _{OL} = 18 mA	2.3 to 2.7			0.2		
			2.3			0.4		
			2.3			0.6		
I _{OL} = 100 μA I _{OL} = 6 mA	1.65 to 2.3			0.2				
	1.65			0.3				
I _{OL} = 100 μA I _{OL} = 2 mA	1.4 to 1.6			0.2				
	1.4			0.35				
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	1.4 to 3.6			±5.0	μA	
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.4 to 3.6			±10	μA	
I _{OFF1}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0			10	μA	
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 8)	1.4 to 3.6			20	μA	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 to 3.6			750	μA	

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.5	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	8.4		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	16.8		Figures 5, 6
t _{PZL} , t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	4.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	5.6		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t _{PLZ} , t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.6	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.0		
			1.8 ± 0.15	1.5	7.2		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	14.4		Figures 5, 7, 8
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 10)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		

Note 9: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.3	V
			2.5	0.7	
			3.3	1.0	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.3	V
			2.5	-0.7	
			3.3	-1.0	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.3	V
			2.5	1.7	
			3.3	2.0	
Capacitance					
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
C _{IN}	Input Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V		6.0	pF
C _{IO}	Input/Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V		7.0	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V		20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)

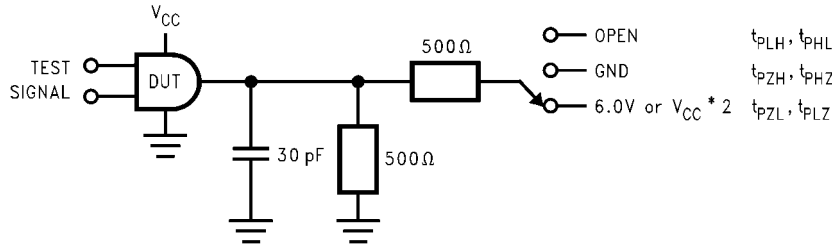


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3V \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

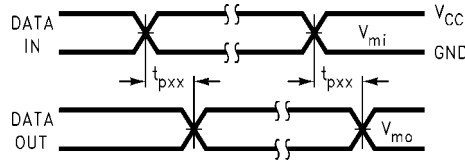


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

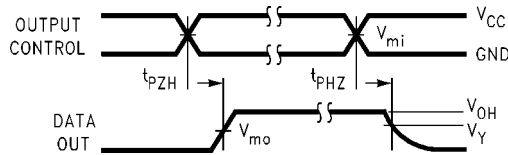


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

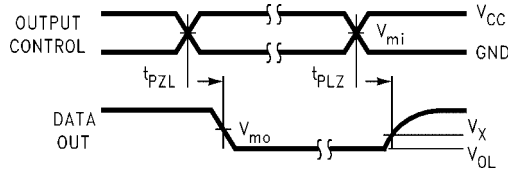
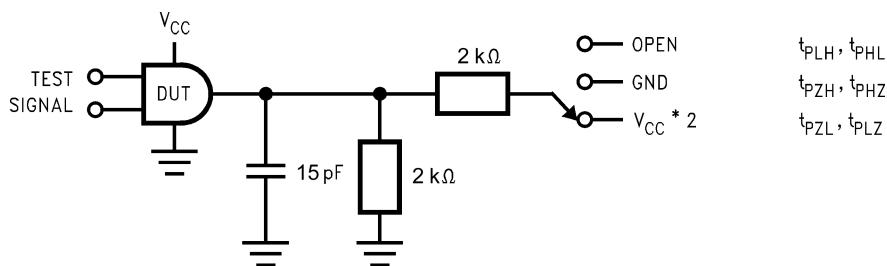


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5 \pm 0.1V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} * 2$ at $V_{CC} = 1.5V \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 5. AC Test Circuit

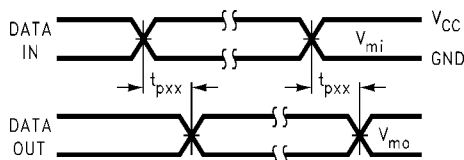


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

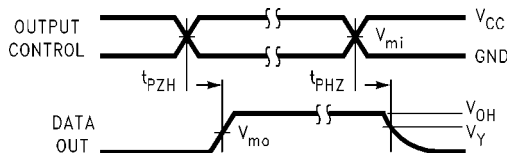


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

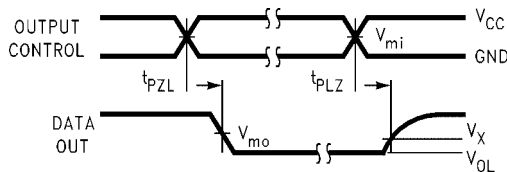


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

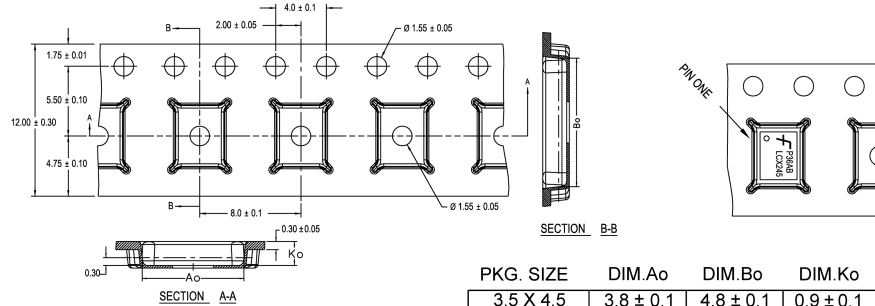
Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



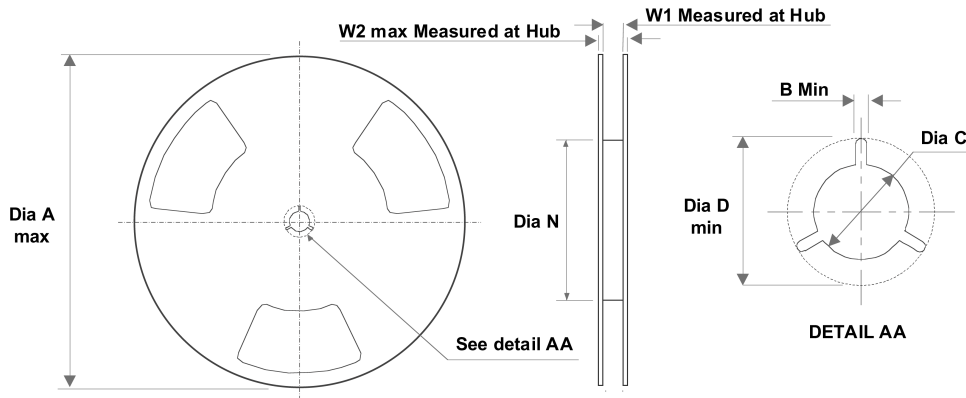
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

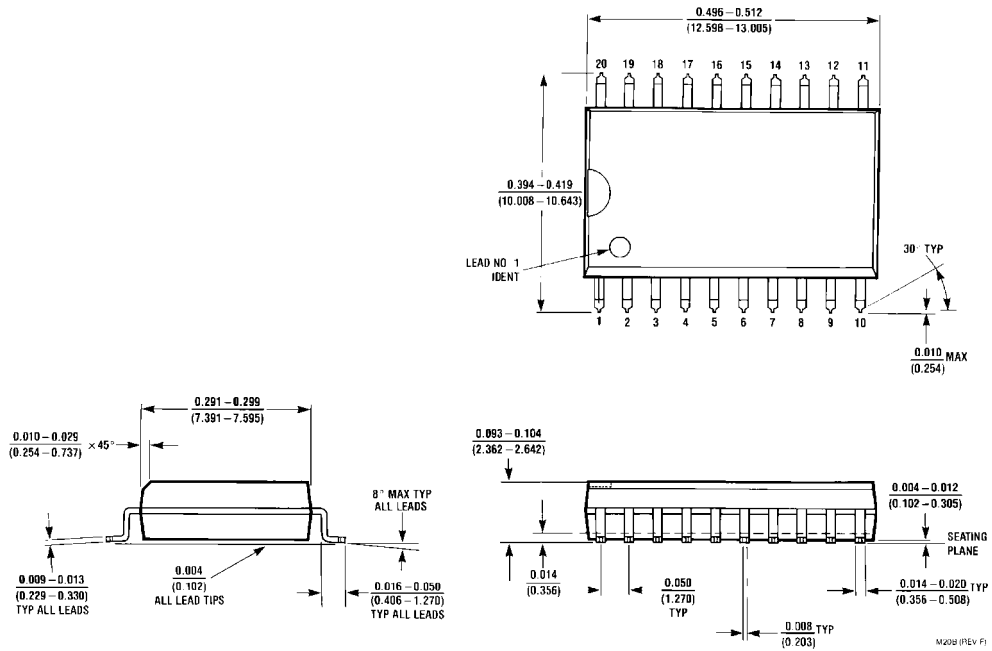
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

